

CLAIMS

What is claimed is:

- 1 1. A fabrication method for a non-volatile memory device, said method
2 comprising:
3 providing a semiconductor substrate comprising a dielectric layer formed on thereon,
4 an insulating composite layer formed on said dielectric layer;
5 forming a patterned protective patterning layer and a patterned first sacrificial layer on
6 said insulating composite layer;
7 trimming said protective patterning layer;
8 patterning said first sacrificial layer by using said protective patterning layer as
9 masks, wherein said first sacrificial layer comprises an opening that exposes said insulating
10 composite layer;
11 removing said protective patterning layer;
12 filling a second sacrificial layer in said opening of said first sacrificial layer;
13 patterning said first sacrificial layer and said insulating composite layer by using said
14 second sacrificial layer as masks and exposing said dielectric layer;
15 removing said second sacrificial layer; and
16 forming a control gate on said composite layer.
- 1 2. The method according to claim 1, wherein said dielectric layer is a silicon
2 dioxide layer.
- 1 3. The method according to claim 1, wherein said insulating composite layer is
2 formed of a silicon dioxide layer and a silicon nitride layer.
- 1 4. The method according to claim 1, wherein said first sacrificial layer a
2 polysilicon layer.

1 5. The method according to claim 1, wherein said second sacrificial layer is a
2 silicon nitride layer.

1 6. The method according to claim 1, wherein said control gate is a polysilicon
2 gate.

1 7. The method according to claim 1, wherein said protective patterning layer is a
2 photoresist layer.

1 8. A method for making a twin bit cell memory device, comprising the steps of:
2 forming on a substrate a tunnel dielectric layer, an insulating charge-trapping layer

3 overlying the tunnel dielectric layer, and a second dielectric layer overlying the charge -
4 trapping layer;

5 forming on said substrate a first patterned sacrificial material overlying said second
6 dielectric layer;

7 using at least said first patterned sacrificial material as a mask, introducing impurities
8 into said substrate;

9 filling openings in said first patterned sacrificial material with a second sacrificial
10 material;

11 removing said first patterned sacrificial material to expose portions of said second
12 dielectric layer through said second sacrificial material;

13 using said second sacrificial material as a mask, opening through-holes in said
14 exposed portions of said second dielectric layer and portions of said charge-trapping layer
15 underlying said exposed portions of said second dielectric layer;

16 removing said second sacrificial material; and

17 forming control gates overlying said second dielectric layer and extending over said
18 through-holes.

1 9. A method according to claim 8, further comprising the step of widening said
2 openings in said first patterned sacrificial material after said step of introducing impurities
3 and before said step of filling openings in said first patterned sacrificial material.

1 10. A method according to claim 9, wherein said first patterned sacrificial material
2 comprises a first sublayer of sacrificial material and a photoresist superposing said first
3 sublayer of sacrificial material, and wherein said step of widening said openings comprises
4 the steps of:

5 trimming said photoresist; and
6 using said photoresist as a mask, re-patterning said first sublayer of sacrificial
7 material.

1 11. A method according to claim 8, wherein said control gates formed in said step
2 of forming control gates also fill said through-holes.

1 12. A method according to claim 8, wherein said tunnel dielectric layer comprises
2 silicon dioxide.

1 13. A method according to claim 8, wherein said second dielectric layer comprises
2 silicon dioxide and said charge-trapping layer comprises silicon nitride.

1 14. A method according to claim 8, wherein said first sacrificial material
2 comprises polysilicon.

1 15. A method according to claim 8, wherein said second sacrificial material
2 comprises silicon nitride.

1 16. A method according to claim 8, wherein said control gates comprise
2 polysilicon.